AMENDMENTS TO THE CLAIMS

1. (Currently amended): A method of reducing power consumption of a clocked circuit containing a plurality of latches, the method comprising the steps of:

locating, within the plurality of latches, a first latch in the clocked circuit having more than a predetermined particular positive slack period, said first latch consuming a first amount of power;

determining availability of a second latch having more than a zero slack period and less than said particular slack period, said second latch consuming a second amount of power which is less than said first amount of power; and

replacing the first latch with the available second latch.

2. (Currently amended): The method as recited in claim 1, wherein the clocked circuit also contains a plurality of local clock buffers, further comprising:

locating, within the clocked circuit, one or more local clock buffers within the plurality of local clock buffers ~~buffer~~, wherein a first clock buffer has a reduced clock load;

determining the availability of a second local clock buffer, wherein the second local clock buffer consumes less ~~drives a lower~~ power [[load]]; and

replacing the first local clock buffer with the available second local clock buffer.

3. (Original): The method as recited in claim 2, wherein the first local clock buffer is a high clock power local clock buffer.

4. (Original): The method as recited in claim 2, wherein the second local clock buffer is a low clock power local clock buffer.

5. (Original): The method as recited in claim 1, wherein replacing the first latch with the second latch forms a modified clocked circuit and further comprising:

testing the modified clock circuit; and

responsive to the modified clock circuit failing the test, inserting the first latch back into the clocked circuit.

6. (Original): The method as recited in claim 5, wherein a timing test tests the modified clock circuit.

7. (Original): The method as recited in claim 1, wherein the first latch is a high power consumption latch.

8. (Original): The method as recited in claim 1, wherein the plurality of latches is a plurality of high power consumption latches.

9. (Original): The method as recited in claim 1, wherein the second latch is a low power consumption latch.

10. (Original): The method of claim 1, wherein the predetermined slack period is at least one of an input slack period and an output slack period.

11. (Original): The method as recited in claim 10, wherein the input slack period is greater than 100 picoseconds.

12. (Original): The method as recited in claim 10, wherein the output slack period is greater than 300 picoseconds.

13. (Currently amended): An apparatus for reducing power consumption of a clocked circuit containing a plurality of latches, comprising:

a first latch;

a timing device; and

a second latch, wherein the first latch is located in the clocked circuit having more than a predetermined slack period by the timing device, availability of the second latch

having more than a zero slack period is determined by the timing device, and the first latch being [[is]] replaced with the available second latch.

14. (Original): The apparatus as recited in claim 13, wherein the first latch is a high power consumption latch.

15. (Original): The apparatus as recited in claim 13, wherein the second latch is a low power consumption latch.

16. (Currently amended): An apparatus for reducing power consumption of a clocked circuit containing a plurality of latches, comprising:

locating means for locating, within the plurality of latches, a first latch in the clocked circuit having more than a predetermined particular positive slack period, said first latch consuming a first amount of power;

determining means for determining availability of a second latch having more than zero slack period and less than said particular slack period, said second latch consuming a second amount of power which is less than said first amount of power; and

replacing means for replacing the first latch with the available second latch.

17. (Currently amended): The apparatus as recited in claim 16, wherein the clocked circuit also contains a plurality of local clock buffers, further comprising:

locating means for locating, within the clocked circuit, one or more local clock buffers within the plurality of local clock buffers ~~buffer~~, wherein a first local clock buffer has a reduced clock load;

determining means for determining the availability of a second local clock buffer, wherein the second local clock buffer consumes less ~~drives a lower~~ power [[load]]; and

replacing means for replacing the first local clock buffer with the available second local clock buffer.

18. (Original): The apparatus as recited in claim 17, wherein the first local clock buffer is a high clock power local clock buffer.

19. (Original): The apparatus as recited in claim 17, wherein the second local clock buffer is a low clock power local clock buffer.

20. (Original): The apparatus as recited in claim 16, wherein replacing the first latch with the second latch forms a modified clocked circuit and further comprising:

testing means for testing the modified clock circuit; and

inserting means, responsive to the modified clock circuit failing the test, for inserting the first latch back into the clocked circuit.

21. (Original): The apparatus as recited in claim 20, wherein a timing test tests the modified clock circuit.

22. (Original): The apparatus as recited in claim 16, wherein the first latch is a high power consumption latch.

23. (Original): The apparatus as recited in claim 16, wherein the plurality of latches is a plurality of high power consumption latches.

24. (Original): The apparatus as recited in claim 16, wherein the second latch is a low power consumption latch.

25. (Original): The apparatus as recited in claim 16, wherein the predetermined slack period is at least one of an input slack period and an output slack period.

26. (Original): The apparatus as recited in claim 25, wherein the input slack period is greater than 100 picoseconds.

27. (Original): The apparatus as recited in claim 25, wherein the output slack period is greater than 300 picoseconds.